

# LM301A, LM201A, LM201AV

## Operational Amplifiers, Non-Compensated, Single

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/ $\mu$ s can be obtained.

### Features

- Low Input Offset Current: 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics
- Pb-Free Packages are Available

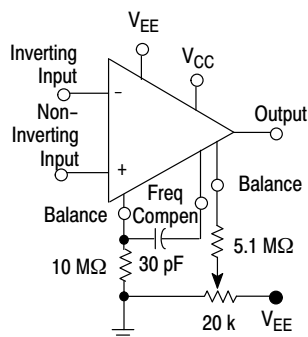


Figure 1. Standard Compensation and Offset Balancing Circuit

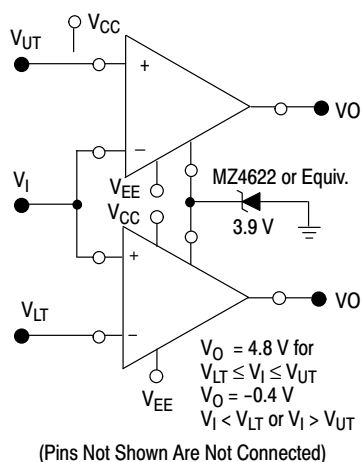


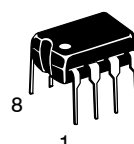
Figure 2. Double-Ended Limit Detector



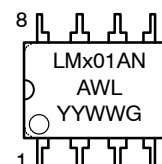
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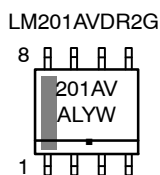
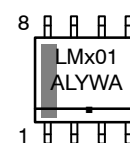
### MARKING DIAGRAMS



PDIP-8  
N SUFFIX  
CASE 626

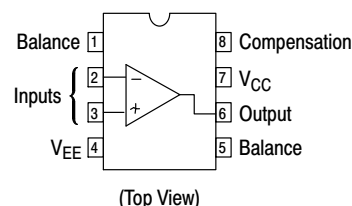


SOIC-8  
D SUFFIX  
CASE 751



x = 2 or 3  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package  
▪ = Pb-Free Package

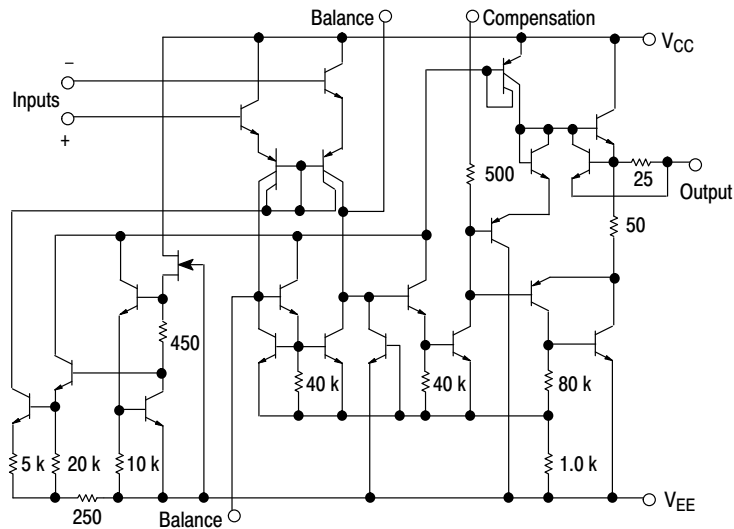
### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# LM301A, LM201A, LM201AV



**Figure 3. Representative Circuit Schematic**

## ORDERING INFORMATION

| Device      | Package             | Shipping <sup>†</sup> |
|-------------|---------------------|-----------------------|
| LM301ADG    | SOIC-8<br>(Pb-Free) | 98 Units/Rail         |
| LM301ADR2G  | SOIC-8<br>(Pb-Free) | 2500 Tape & Reel      |
| LM301AN     | PDIP-8              | 50 Units/Rail         |
| LM301ANG    | PDIP-8<br>(Pb-Free) | 50 Units/Rail         |
| LM201ADG    | SOIC-8<br>(Pb-Free) | 98 Units/Rail         |
| LM201ADR2G  | SOIC-8<br>(Pb-Free) | 2500 Tape & Reel      |
| LM201AN     | PDIP-8              | 50 Units/Rail         |
| LM201ANG    | PDIP-8<br>(Pb-Free) | 50 Units/Rail         |
| LM201AVDR2G | SOIC-8<br>(Pb-Free) | 2500 Tape & Reel      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# LM301A, LM201A, LM201AV

## MAXIMUM RATINGS

| Rating                                                                                                           | Symbol           | Value           |                 |              | Unit                       |
|------------------------------------------------------------------------------------------------------------------|------------------|-----------------|-----------------|--------------|----------------------------|
|                                                                                                                  |                  | LM201A          | LM201AV         | LM301A       |                            |
| Power Supply Voltage                                                                                             | $V_{CC}, V_{EE}$ | $\pm 22$        | $\pm 22$        | $\pm 18$     | Vdc                        |
| Input Differential Voltage                                                                                       | $V_{ID}$         | $\pm 30$        |                 |              | V                          |
| Input Common Mode Range (Note 1)                                                                                 | $V_{ICR}$        | $\pm 15$        |                 |              | V                          |
| Output Short Circuit Duration                                                                                    | $t_{SC}$         | Continuous      |                 |              |                            |
| Power Dissipation (Package Limitation)<br>Plastic Dual-In-Line Package<br>Derate above $T_A = +25^\circ\text{C}$ | $P_D$            | 625<br>5.0      | 625<br>5.0      | 625<br>5.0   | mW<br>mW/ $^\circ\text{C}$ |
| Operating Ambient Temperature Range                                                                              | $T_A$            | $-25$ to $+85$  | $-40$ to $+105$ | $0$ to $+70$ | $^\circ\text{C}$           |
| Storage Temperature Range                                                                                        | $T_{stg}$        | $-65$ to $+150$ |                 |              | $^\circ\text{C}$           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**ELECTRICAL CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$ , unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from  $\pm 5.0$  V to  $\pm 20$  V for the LM201A and LM201AV, and from  $\pm 5.0$  V to  $\pm 15$  V for the LM301A.

| Characteristic                                                                                        | Symbol           | LM201A / LM201AV |          |          | LM301A |          |          | Unit       |
|-------------------------------------------------------------------------------------------------------|------------------|------------------|----------|----------|--------|----------|----------|------------|
|                                                                                                       |                  | Min              | Typ      | Max      | Min    | Typ      | Max      |            |
| Input Offset Voltage ( $R_S \leq 50$ k $\Omega$ )                                                     | $V_{IO}$         | –                | 0.7      | 2.0      | –      | 2.0      | 7.5      | mV         |
| Input Offset Current                                                                                  | $I_{IO}$         | –                | 1.5      | 10       | –      | 3.0      | 50       | nA         |
| Input Bias Current                                                                                    | $I_{IB}$         | –                | 30       | 75       | –      | 70       | 250      | nA         |
| Input Resistance                                                                                      | $r_i$            | 1.5              | 4.0      | –        | 0.5    | 2.0      | –        | M $\Omega$ |
| Supply Current<br>$V_{CC}/V_{EE} = \pm 20$ V<br>$V_{CC}/V_{EE} = \pm 15$ V                            | $I_{CC}, I_{EE}$ | –<br>–           | 1.8<br>– | 3.0<br>– | –<br>– | –<br>1.8 | –<br>3.0 | mA         |
| Large Signal Voltage Gain<br>( $V_{CC}/V_{EE} = \pm 15$ V, $V_O = \pm 10$ V, $R_L > 2.0$ k $\Omega$ ) | $A_V$            | 50               | 160      | –        | 25     | 160      | –        | V/mV       |

The following specifications apply over the operating temperature range.

|                                                                                                                                                                       |                          |                      |                      |            |                      |                      |            |                              |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------------|----------------------|------------|----------------------|----------------------|------------|------------------------------|
| Input Offset Voltage ( $R_S \leq 50$ k $\Omega$ )                                                                                                                     | $V_{IO}$                 | –                    | –                    | 3.0        | –                    | –                    | 10         | mV                           |
| Input Offset Current                                                                                                                                                  | $I_{IO}$                 | –                    | –                    | 20         | –                    | –                    | 70         | nA                           |
| Avg Temperature Coefficient of Input Offset Voltage (Note 2)<br>$T_A(\text{min}) \leq T_A \leq T_A(\text{max})$                                                       | $\Delta V_{IO}/\Delta T$ | –                    | 3.0                  | 15         | –                    | 6.0                  | 30         | $\mu\text{V}/^\circ\text{C}$ |
| Avg Temperature Coefficient of Input Offset Current (Note 2)<br>$+25^\circ\text{C} \leq T_A \leq T_A(\text{max})$<br>$T_A(\text{min}) \leq T_A \leq 25^\circ\text{C}$ | $\Delta I_{IO}/\Delta T$ | –<br>–               | 0.01<br>0.02         | 0.1<br>0.2 | –<br>–               | 0.01<br>0.02         | 0.3<br>0.6 | nA/ $^\circ\text{C}$         |
| Input Bias Current                                                                                                                                                    | $I_{IB}$                 | –                    | –                    | 100        | –                    | –                    | 300        | nA                           |
| Large Signal Voltage Gain<br>( $V_{CC}/V_{EE} = \pm 15$ V, $V_O = \pm 10$ V, $R_L > 2.0$ k $\Omega$ )                                                                 | $A_{VOL}$                | 25                   | –                    | –          | 15                   | –                    | –          | V/mV                         |
| Input Voltage Range<br>$V_{CC}/V_{EE} = \pm 20$ V<br>$V_{CC}/V_{EE} = \pm 15$ V                                                                                       | $V_{ICR}$                | $-15$<br>–           | –<br>–               | $+15$<br>– | –<br>$-12$           | –<br>–               | –<br>$+12$ | V                            |
| Common Mode Rejection ( $R_S \leq 50$ k $\Omega$ )                                                                                                                    | CMR                      | 80                   | 96                   | –          | 70                   | 90                   | –          | dB                           |
| Supply Voltage Rejection ( $R_S \leq 50$ k $\Omega$ )                                                                                                                 | PSR                      | 80                   | 96                   | –          | 70                   | 96                   | –          | dB                           |
| Output Voltage Swing<br>( $V_{CC}/V_{EE} = \pm 15$ V, $R_L = \pm 10$ k $\Omega$ , $R_L > 2.0$ k $\Omega$ )                                                            | $V_O$                    | $\pm 12$<br>$\pm 10$ | $\pm 14$<br>$\pm 13$ | –<br>–     | $\pm 12$<br>$\pm 10$ | $\pm 14$<br>$\pm 13$ | –<br>–     | V                            |
| Supply Currents ( $T_A = T_A(\text{max})$ , $V_{CC}/V_{EE} = \pm 20$ V)                                                                                               | $I_{CC}, I_{EE}$         | –                    | 1.2                  | 2.5        | –                    | –                    | –          | mA                           |

- For supply voltages less than  $\pm 15$  V, the absolute maximum input voltage is equal to the supply voltage.
- Guaranteed by design.

# LM301A, LM201A, LM201AV

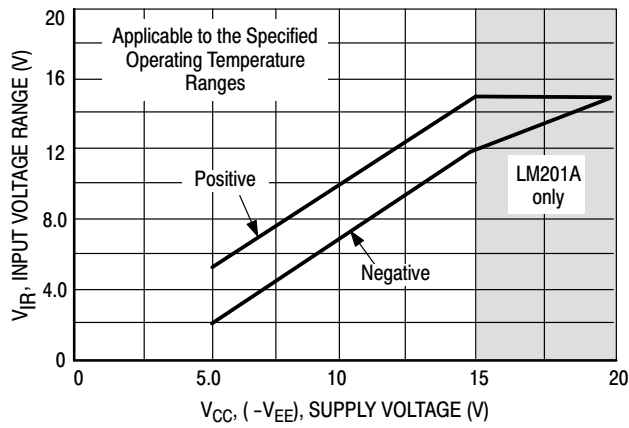


Figure 4. Minimum Input Voltage Range

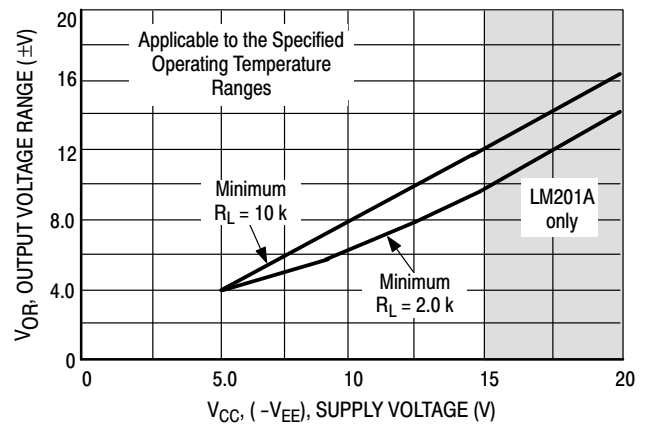


Figure 5. Minimum Output Voltage Swing

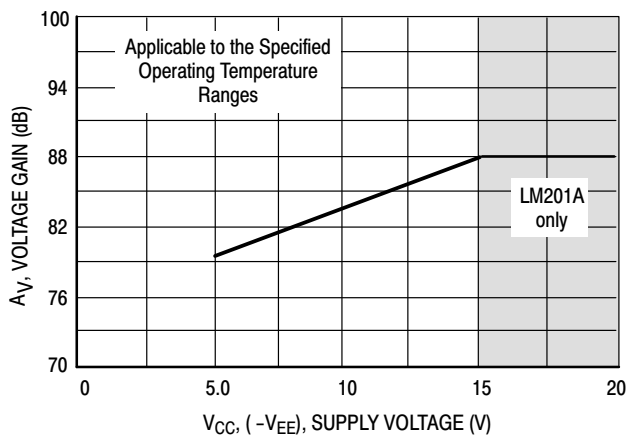


Figure 6. Minimum Voltage Gain

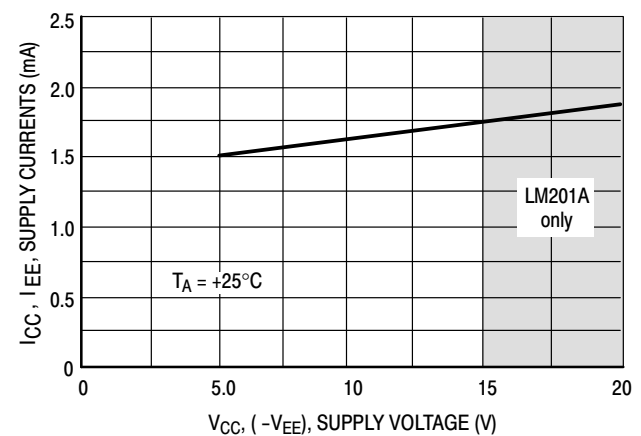


Figure 7. Typical Supply Currents

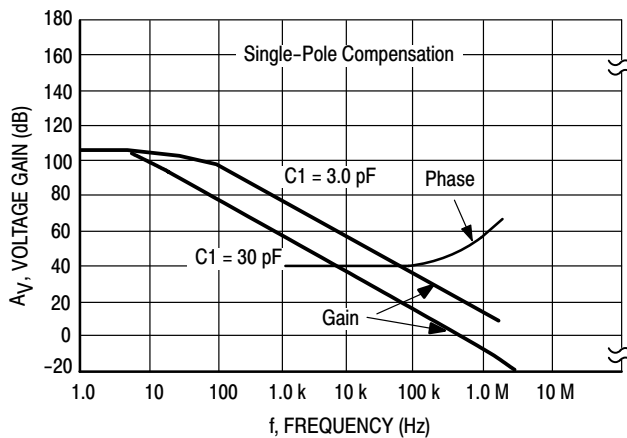


Figure 8. Open Loop Frequency Response

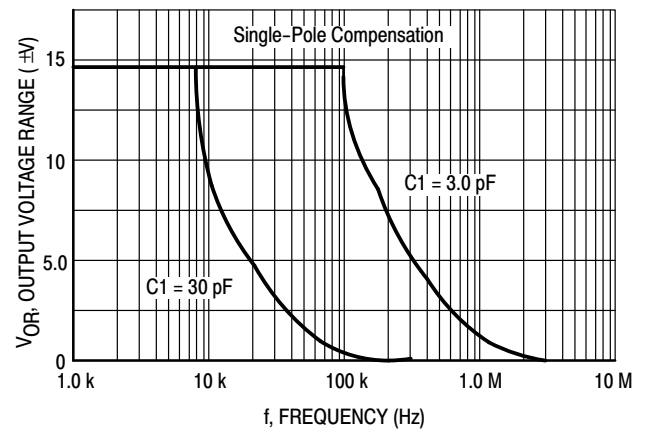


Figure 9. Large Signal Frequency Response

# LM301A, LM201A, LM201AV

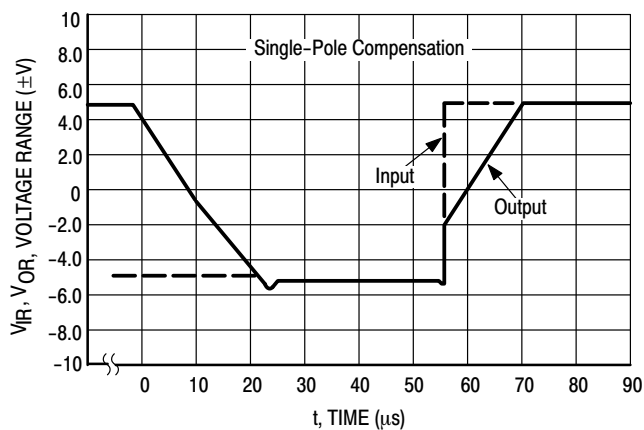


Figure 10. Voltage Follower Pulse Response

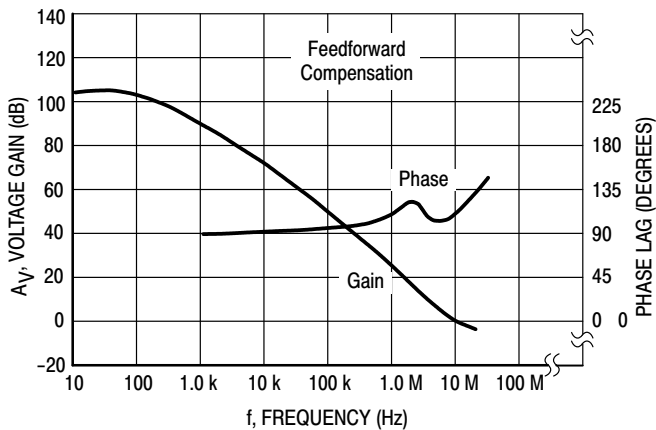


Figure 11. Open Loop Frequency Response

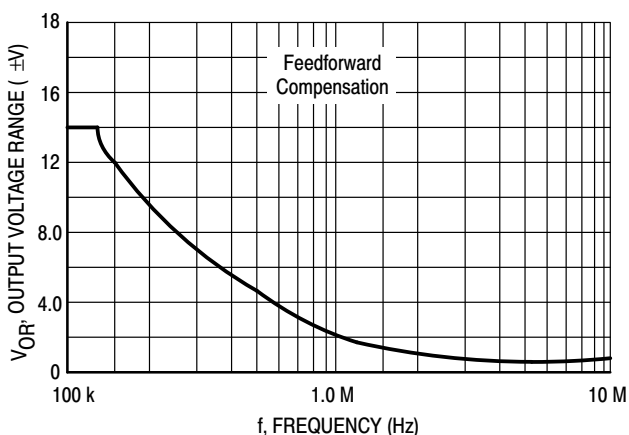


Figure 12. Large Signal Frequency Response

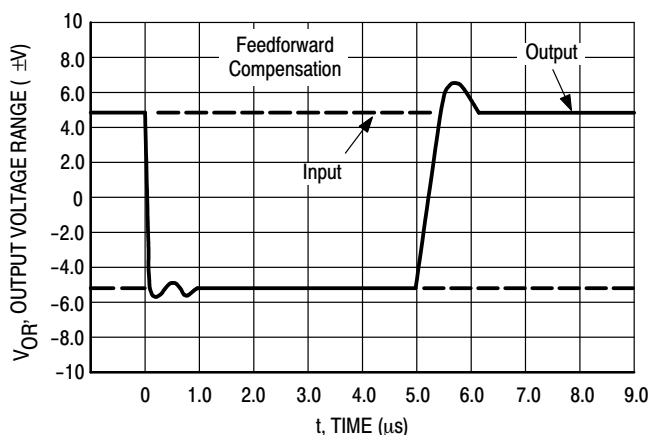


Figure 13. Inverter Pulse Response

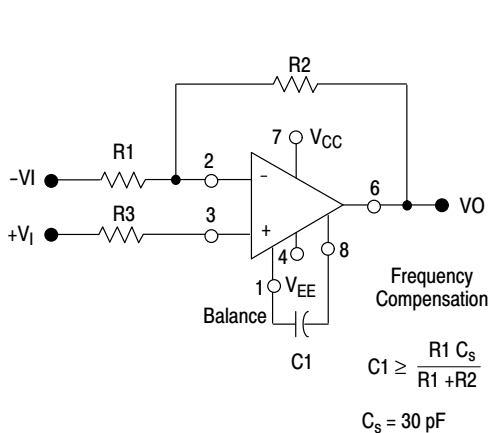


Figure 14. Single-Pole Compensation

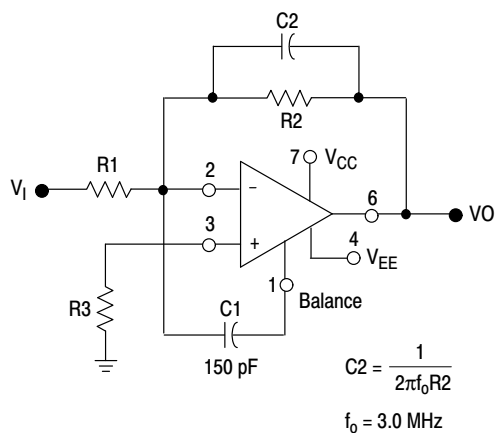


Figure 15. Feedforward Compensation

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

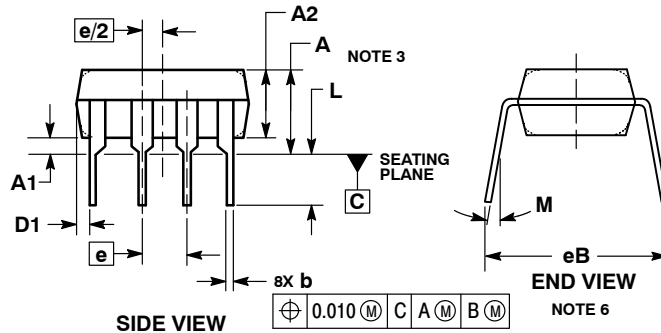
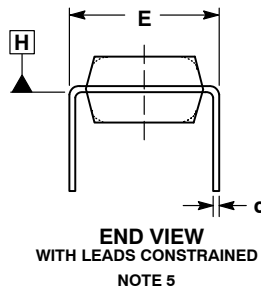
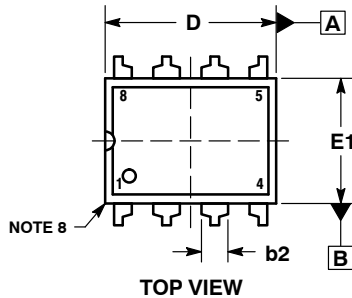
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SCALE 1:1

PDIP-8  
CASE 626-05  
ISSUE P

DATE 22 APR 2015

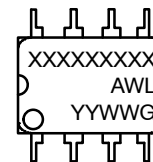


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | ---       | 0.210 | ---         | 5.33  |
| A1  | 0.015     | ---   | 0.38        | ---   |
| A2  | 0.115     | 0.195 | 2.92        | 4.95  |
| b   | 0.014     | 0.022 | 0.35        | 0.56  |
| b2  | 0.060 TYP |       | 1.52 TYP    |       |
| C   | 0.008     | 0.014 | 0.20        | 0.36  |
| D   | 0.355     | 0.400 | 9.02        | 10.16 |
| D1  | 0.005     | ---   | 0.13        | ---   |
| E   | 0.300     | 0.325 | 7.62        | 8.26  |
| E1  | 0.240     | 0.280 | 6.10        | 7.11  |
| e   | 0.100 BSC |       | 2.54 BSC    |       |
| eB  | ---       | 0.430 | ---         | 10.92 |
| L   | 0.115     | 0.150 | 2.92        | 3.81  |
| M   | ---       | 10°   | ---         | 10°   |

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### STYLE 1:

- PIN 1: AC IN  
2. DC + IN  
3. DC - IN  
4. AC IN  
5. GROUND  
6. OUTPUT  
7. AUXILIARY  
8. V<sub>CC</sub>

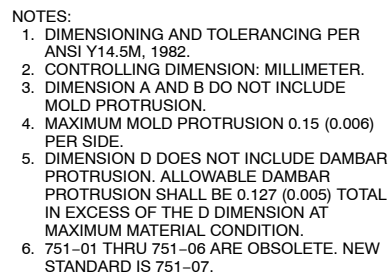
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| <b>DESCRIPTION:</b>     | <b>PDIP-8</b>      | <b>PAGE 1 OF 1</b>                                                                                                                                                                  |

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# onsemi

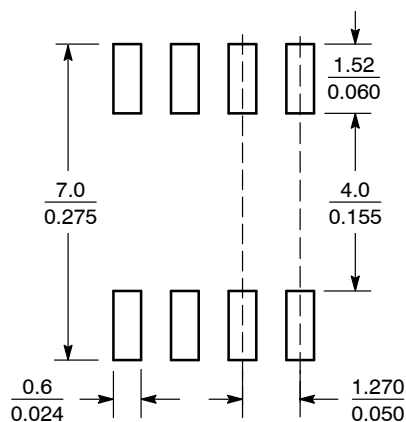


DATE 16 FEB 2011

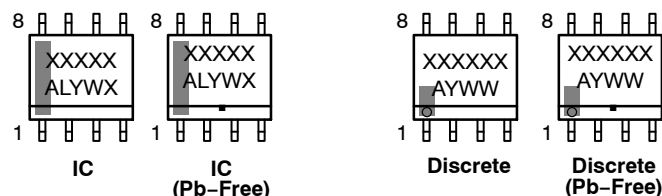


| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

## SOLDERING FOOTPRINT\*



SCALE 6:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

|                         |                    |                                                                                                                                                                                     |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| <b>DESCRIPTION:</b>     | <b>SOIC-8 NB</b>   | <b>PAGE 1 OF 2</b>                                                                                                                                                                  |

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
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